

ENGIN 112 - Homework 8

Due Wednesday, November 24

1. Mano; Problem 5.5.
2. Mano; Problem 5.6.
3. In this problem, you will design a simple four clock pulse timer circuit. In addition to the clock input, the timer has a Restart input (R), three data outputs (ABC) which indicate the count, and one beeper output (D). The behavior of the circuit is as follows:
 - *Idle Mode* The timer output is $ABC=100$ and the beeper is off ($D=0$) as long as $R=0$. If $R=1$ on any clock edge in this mode, the counter goes into the
 - *Restart/Hold Mode* The timer output is $ABC=000$ and the beeper is off ($D=0$) as long as $R=1$. If $R=0$ on any clock edge in this mode, the timer goes into the
 - *Counting Mode* Provided that the counter is not restarted (i.e. provided that $R=0$), the timer goes through the following sequence of data and beeper outputs (one full clock pulse each):

A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1

and then returns to the *Idle* mode. If $R=1$ on any clock edge in this mode, the timer goes into the *Restart/Hold* mode.

Use D-flops, AND gates, OR gates, and inverters to design a Moore machine that performs this function. No more than 3 D-type flip flops should be used. Carry out your solution as follows:

- (a) How many states does this machine have? Make a list of these states, giving each a label and a verbal description. How many bits are required to specify all states? Name the state bits and assign values to each for every state.
- (b) Construct a complete state table for this machine, including all inputs, outputs, and states. Include any dont-care conditions.
- (c) Construct a state diagram for this machine.
- (d) How many signals must be generated by combinational logic for this machine? What are they? Use Karnaugh maps to obtain minimized Boolean expressions for combinational circuits which will generate these signals, and draw a circuit diagram for each circuit.
- (e) Draw a complete circuit diagram for your state machine, showing all inputs and outputs, flip flops, combinational circuits, and interconnects. You can represent each of your combinational circuits from part (d) as a box in this diagram, but make sure that the inputs and outputs are clearly labeled on each box.

Note that all problems from the Mano textbook are from the 4th Edition. The “HDL” parts of these problems are *not* assigned.